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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/077,207	05/26/1998	SATOSHI INOUE	JAO40840	5738

25944 7590 12/31/2003

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/077,207	INOUE, SATOSHI	
	Examin r	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44,47-56,59,60,62 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *44,47-49,59,60,62 and 63* is/are allowed.

6)☒ Claim(s) *50-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

This non-final Office Action is in response to the amendment filed October 31, 2003.

As a preliminary matter, although another interview seems unnecessary in this case, a request for an interview will be granted if the interview is held before the applicant files a response.

Claims 52-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claim 52 is incorrect in reciting: "said thin film transistors having an inverse conductivity type from each other, adjacent source-drain regions of said thin film transistors being connected; wherein said radiating extension is formed in a region opposed to said source-drain wiring layer, said source-drain wiring layer connecting the adjacent source-drain regions of said thin film transistors," because the disclosed radiating extension is not formed in a region opposed to the source-drain wiring layer connecting the adjacent source-drain regions of said thin film transistors having inverse conductivity type from each other. See Fig. 6, for example, and note that the radiating extensions 125A and 125B are not formed in a region opposed to the source-drain wiring layer 803 connecting the adjacent source-drain regions of said thin film transistors 1A and 1B having an inverse conductivity type from each other. Rather, the radiating extensions 125A and 125B are formed in a region opposed to the source-drain wiring layers 802 and 801 connecting adjacent source-drain regions 12A and 12B of adjacent thin film transistors having the same conductivity type.

Independent claim 53 is indefinite because "the component parts" and "said thin film transistors" lack antecedent basis. Claim 53 should be amended to provide antecedent basis for "said thin film transistors" and "the component parts" (note independent claims 50-52 in this regard).

Independent claim 53 is also unclear in reciting: "forming a liquid crystal display device comprising an active matrix substrate on which a driving circuit including a CMOS inverter [sic]," particularly insofar as device claim 53 already recites: "A liquid crystal display device comprising: an active matrix substrate; a driving circuit formed on the active matrix substrate and including a CMOS inverter circuit." Claim 53's "forming" clause should apparently be deleted.

Independent claim 54 is indefinite because "the component parts" lack antecedent basis. Claim 54 should be amended to provide antecedent basis for "the component parts" (note independent claims 50-52 in this regard).

Independent claim 55 is indefinite because "the component parts" and "said thin film transistors" lack antecedent basis. Claim 55 should be amended to provide antecedent basis for "said thin film transistors" and "the component parts" (note independent claims 50-52 in this regard).

Independent claim 55 is also unclear in reciting: "forming a liquid crystal display device comprising an active matrix substrate on which a driving circuit including a CMOS inverter [sic]," particularly insofar as device claim 55 already recites: "A liquid crystal display device comprising: an active matrix substrate; a driving circuit formed on

the active matrix substrate and including a CMOS inverter circuit." Claim 55's "forming" clause should apparently be deleted.

Independent claim 56 is indefinite because "the component parts" lack antecedent basis. Claim 56 should be amended to provide antecedent basis for "the component parts" (note independent claims 50-52 in this regard).

Claims 50-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (newly cited United States Patent 6,144,041 – hereafter Yamazaki).

With respect to independent claim 50, Yamazaki discloses (see the entire patent, particularly the Figs. 7-8 disclosure) a CMOS inverter circuit, comprising: two thin film transistors 717 and 718, each thin film transistor including a plurality of component parts that include: a channel region (817 and 814); a gate electrode (811 and 810) opposed to the channel region, a gate insulating film provided between the channel region and the gate electrode; a source-drain region (816/818 and 813/815) connected to said channel region; a source-drain wiring layer (823-825) electrically connected to said source-drain region; and a gate wiring layer electrically connected to said gate electrode (the Fig. 7B wiring connecting the two gate electrodes), at least one of the component parts (the source-drain region) being formed from a conductive film or a semiconductor film and being provided with a radiating extension extending outwardly from the at least one component part, said radiating extension extending from both sides of said source-drain region (see Fig. 7B), said thin film transistors 717 and 718 having an inverse conductivity type from each other, adjacent source-drain regions 815 and 816 of said thin film transistors being connected.

Claim 50 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

With respect to independent claim 51, Yamazaki discloses (see the entire patent, particularly the Figs. 7-8 disclosure) a CMOS inverter circuit, comprising: two thin film transistors 717 and 718, each thin film transistor including a plurality of component parts that include: a channel region (817 and 814); a gate electrode (811 and 810) opposed to the channel region, a gate insulating film provided between the channel region and the gate electrode; a source-drain region (816/818 and 813/815) connected to said channel region; a source-drain wiring layer (823-825) electrically connected to said source-drain region; and a gate wiring layer electrically connected to said gate electrode (the Fig. 7B wiring connecting the two gate electrodes), at least one of the component parts (the source-drain region) being formed from a conductive film or a semiconductor film and being provided with a radiating extension extending outwardly from the at least one component part, wherein said radiating extension extends from both sides of said source-drain region (see Fig. 7B), said thin film transistors 717 and 718 having an inverse conductivity type from each other, adjacent source-drain regions 815 and 816 of said thin film transistors being connected, wherein said radiating extension is provided with a conductivity by using an impurity identical to an impurity of said source-drain region to which said radiating extension is connected (i.e., Yamazaki's extended source-drain regions are uniform).

Claim 51 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

With respect to independent claim 52, Yamazaki discloses (see the entire patent, particularly the Figs. 7-8 disclosure) a CMOS inverter circuit, comprising: two thin film transistors 717 and 718, each thin film transistor including a plurality of component parts that include: a channel region (817 and 814); a gate electrode (811 and 810) opposed to the channel region, a gate insulating film provided between the channel region and the gate electrode; a source-drain region (816/818 and 813/815) connected to said channel region; a source-drain wiring layer (823-825) electrically connected to said source-drain region; and a gate wiring layer electrically connected to said gate electrode (the Fig. 7B wiring connecting the two gate electrodes), at least one of the component parts (the source-drain region) being formed from a conductive film or a semiconductor film and being provided with a radiating extension extends outwardly from the at least one component part, said radiating extension extending from both sides of said source-drain region (see Fig. 7B), said thin film transistors 717 and 718 having an inverse conductivity type from each other, adjacent source-drain regions 815 and 816 of said thin film transistors being connected; wherein said radiating extension is formed in a region opposed to said source-drain wiring layer 824 (see Fig. 7B), said source-drain wiring layer 824 connecting the adjacent source-drain regions of said thin film transistors.

Claim 52 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

With respect to independent claim 53, Yamazaki discloses (see the entire patent, particularly the Figs. 7-8 disclosure) a liquid crystal display device comprising: an active

matrix substrate 701/801; a driving circuit 702/703 formed on the active matrix substrate and including a CMOS inverter circuit, the liquid crystal display device includes [two thin film transistors 717 and 718, each thin film transistor including a plurality of component parts that include]: a channel region (817 and 814); a gate electrode (811 and 810) opposed to the channel region, a gate insulating film provided between the channel region and the gate electrode; a source-drain region (816/818 and 813/815) connected to said channel region; a source-drain wiring layer (823-825) electrically connected to said source-drain region; and a gate wiring layer electrically connected to said gate electrode (the Fig. 7B wiring connecting the two gate electrodes), at least one of the component parts (the source-drain region) being formed from a conductive film or a semiconductor film and being provided with a radiating extension extending outwardly from the at least one component part, wherein said radiating extension extends from both sides of said source-drain region (see Fig. 7B), said thin film transistors 717 and 718 having an inverse conductivity type from each other, adjacent source-drain regions 815 and 816 of said thin film transistors being connected.

Claim 53, at least insofar as understood, is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

With respect to independent claim 54, Yamazaki discloses (see the entire patent, particularly the Figs. 7-8 disclosure) an electronic apparatus comprising a CMOS inverter circuit, the CMOS inverter circuit having two thin film transistors 717 and 718, each thin film transistor [including a plurality of component parts] that include: a channel region (817 and 814); a gate electrode (811 and 810) opposed to the channel

region, a gate insulating film provided between the channel region and the gate electrode; a source-drain region (816/818 and 813/815) connected to said channel region; a source-drain wiring layer (823-825) electrically connected to said source-drain region; and a gate wiring layer electrically connected to said gate electrode (the Fig. 7B wiring connecting the two gate electrodes), at least one of the component parts (the source-drain region) being formed from a conductive film or a semiconductor film and being provided with a radiating extension extending outwardly from the at least one component part, wherein said radiating extension extends from both sides of said source-drain region (see Fig. 7B), said thin film transistors 717 and 718 having an inverse conductivity type from each other, adjacent source-drain regions 815 and 816 of said thin film transistors being connected; [the] electronic apparatus comprising [the] CMOS inverter circuit.

Claim 54, at least insofar as understood, is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

With respect to independent claim 55, Yamazaki discloses (see the entire patent, particularly the Figs. 7-8 disclosure) a liquid crystal display device comprising: an active matrix substrate 701/801; a driving circuit 702/703 formed on the active matrix substrate and including a CMOS inverter circuit, the liquid crystal display device includes [two thin film transistors 717 and 718, each thin film transistor including a plurality of component parts that include]: a channel region (817 and 814); a gate electrode (811 and 810) opposed to the channel region, a gate insulating film provided between the channel region and the gate electrode; a source-drain region (816/818 and 813/815) connected

to said channel region; a source-drain wiring layer (823-825) electrically connected to said source-drain region; and a gate wiring layer electrically connected to said gate electrode (the Fig. 7B wiring connecting the two gate electrodes), at least one of the component parts (the source-drain region) being formed from a conductive film or a semiconductor film and being provided with a radiating extension extending outwardly from the at least one component part, wherein said radiating extension extends from both sides of said source-drain region (see Fig. 7B), said thin film transistors 717 and 718 having an inverse conductivity type from each other, adjacent source-drain regions 815 and 816 of said thin film transistors being connected; said plurality of component parts each extending in a longitudinal direction, the radiating extension extending in a direction substantially perpendicular to the longitudinal direction (see Fig. 7B).

Claim 55, at least insofar as understood, is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

With respect to independent claim 56, Yamazaki discloses (see the entire patent, particularly the Figs. 7-8 disclosure) an electronic apparatus comprising a CMOS inverter circuit, the CMOS inverter circuit having two thin film transistors 717 and 718, each thin film transistor [including a plurality of component parts] that include: a channel region (817 and 814); a gate electrode (811 and 810) opposed to the channel region, a gate insulating film provided between the channel region and the gate electrode; a source-drain region (816/818 and 813/815) connected to said channel region; a source-drain wiring layer (823-825) electrically connected to said source-drain region; and a gate wiring layer electrically connected to said gate electrode (the Fig. 7B

wiring connecting the two gate electrodes), at least one of the component parts (the source-drain region) being formed from a conductive film or a semiconductor film and being provided with a radiating extension extending outwardly from the at least one component part, wherein said radiating extension extends from both sides of said source-drain region (see Fig. 7B), said thin film transistors 717 and 718 having an inverse conductivity type from each other, adjacent source-drain regions 815 and 816 of said thin film transistors being connected; [the] electronic apparatus comprising [the] CMOS inverter circuit; said plurality of component parts each extending in a longitudinal direction, the radiating extension extending in a direction substantially perpendicular to the longitudinal direction (see Fig. 7B).

Claim 56, at least insofar as understood, is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

Claims 44, 47-49, 59, 60, 62 and 63 are allowable over the prior art of record.

The prior art of record does not disclose or suggest the allowable thin film transistors taken as a whole, including the plurality of contact holes.

Registered practitioners can telephone the examiner at (703) 308-4939 until January 7, 2004 and then at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (703) 308-0956 until January 2004 and then (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner